varied as a function of the varying of the memory clock frequency. As taught by Jones, one of several different clock frequencies are selected depending upon the total bandwidth required by various functions of the graphics processor. Accordingly, a single variable memory clock signal is disclosed. Its frequency can be varied to vary the clock frequency of the frame buffer memory clock. The memory clock signal of Jones is not divided into a plurality of independent clock signals that are coupled to a number of memory interface circuits for differing processing engines.

As a preliminary matter, Applicants' attorney wishes to thank Examiner Kim for the courtesies extended during the telephone interview of July 30, 2002. As noted in the telephone conference, Applicants were are unable to determine the precise grounds for rejection of Claim 1. For example, as to the claimed memory clock divider circuit, the Office Action appears to cite Jones as teaching the circuit as claimed, citing Fig. 4, but when referring to Jones, the Office Action also appears to refer to Col. 12, Claim 2. However, the Jones patent does not include 12 columns. The Examiner stated that this reference to Col. 12, Claim 2 was an error and should be omitted. Moreover, it appears that the Office Action contradicts itself. On page 3 thereof, 1st paragraph, the Office Action cites Figure 4 of Jones as allegedly showing a memory clock divider circuit that generates divided memory clock output signals as a plurality of independent clock signals to a number of interfaces for processing engines and that activates at least some of the plurality of clock signals in response to received condition data during an active mode. However, in the next paragraph the Office Action states the opposite. The Office Action states, "Jones, Jr. does not show the plurality of corresponding independent clock signals to a number of interface circuits for differing processing engines and selectively activates at least some of the plurality of independent clock signals in response to received condition data during an active mode." The Examiner indicated that Jones allegedly teaches everything of Claim 1 except "selectively" activating some of the independent clock signals. Applicants respectfully submit that the Jones reference is being misinterpreted. During the telephone conference the Examiner indicated that the lines coming out from the comparators in Fig. 4, namely comparators 410, 411 and 412 are allegedly the divided memory clock signals output as a plurality of corresponding independent clock signals that go to a number of memory interface circuits for differing processing engines of a graphics controller. Applicants respectfully submit that Fig. 4 of Jones is

merely "clock control logic" which generates control signals, not divided memory clock, which act as select signals for clocks CLK, CLK/2 and CLK/4 (not shown in Fig. 4).

In fact, Col. 4, states that the comparators 410, 411 and 412 have inputs that are shown coming from a cycle point 44 shown to be a latch. "The other inputs to comparators 410, 411 and 412 are the minimum rates for which the CLK, CLK/2 and CLK/4 signals are respectively required." As such, the outputs to the comparators are <u>control signals</u> also referred to as "clock select signals" which are "control signals" that could be input to a phase locked loop (Col. 4, ll. 48-54). As such, the outputs of the comparators 410, 411 and 412 are not independent clock signals divided from a memory clock but to the contrary, are control signals one of which selects an appropriate clock frequency, namely a clock frequency associated with CLK select 430, CLK/2 select 431 or CLK/4 select 432. As such, the control signals select one clock frequency as the memory clock frequency, according, for example to the table shown in Col. 4. (See, e.g., Col. 4, ll. 17-36). The clock control logic of Fig. 4 carries out the selection of one clock frequency in the table. There is no memory clock generator or dividing circuit shown in Fig. 4. Accordingly, the claims are believed to be in condition for allowance.

Moreover, the Jones reference teaches varying the memory clock frequency to the frame buffer. Jones does not mention controlling the clock, namely a number of corresponding independent clock signals that have been divided through a memory clock divider circuit to a number of interface circuits for differing processing engines of a graphics controller. Accordingly, the claims are also believed to be in condition for allowance for this reason.

Moreover, Applicants claim, among other things, selectively activating at least some of the plurality of independent clock signals in response to received condition data during an active mode. As such, Applicants' invention turns on and off clock signals, namely a plurality of independent clock signals from the memory clock that go to differing graphics processor processing engines in response to received condition data, during an active mode. In contrast, Jones does not appear to teach or suggest shutting off a memory clock but instead varies the frequency of the memory clock. Accordingly, the claims are believed to be in condition for allowance.

In addition, the Office Action cites Houston, Col. 12, Claim 2 and Col. 3, ll. 1-7. However, as noted above, Applicants claim, among other things, selectively activating at least some of the plurality of independent clock signals that are divided from a memory clock in a graphics processor whereas Col. 12, Claim 2 describes, among other things, selecting an identified element of a circuit and reducing the frequency of a clock signal input to the element to a non-zero second frequency from a normal operating frequency. Again, Applicants respectfully note that this does not teach selectively activating at least some of the plurality of independent clock signals that have been divided from a memory clock wherein the independent clock signals go to a number of corresponding interface circuits for differing processing engines of a graphics processor, since, among other things, selectively activating as claimed requires the shutting off of a plurality of independent clock signals to the interface circuits. The cited portion of Houston teaches an opposite approach, namely making it a non-zero frequency. Accordingly, the claims are believed to be in condition for allowance.

In addition, Applicants also respectfully challenge the motivation to combine the teachings of Houston with those of Jones since, among other things, Jones appears to use an opposite approach from that of Houston.

Houston is directed to a system and method for reducing power dissipation in a circuit wherein an element of a circuit is identified and selected and an input to the element is altered to reduce the power dissipated by the element wherein, in particular, a logic component may determine an interval based on expired clock cycles or instructions processed. As such, the logic component evaluates instructions or the executable sequences of operations associated with specific elements. Such elements can then be selected for reduced power dissipation for a duration of the sequence of operations. The logic component may also utilize pattern recognition and pattern matching of a series of instructions as they are handled (see, e.g., Col. 7, ll. 14-62).

The Office Action attempts to combine the teachings of Jones with those of Houston. However, it is unclear which teachings from which reference are being combined. The Office Action states "it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the plurality of corresponding independent clock signals to a number of interface circuits for differing processing engines and selectively activate at least

some of the plurality of independent clock signals in response to received condition data during an active mode as shown in Houston for reducing power without impacting the operation the rest of the circuit." It is not clear which teaching from Jones is allegedly combinable with Houston.

Moreover, Jones teaches away from Houston (and Applicants') claimed invention by, among other things, utilizing a single memory clock signal. It does not teach, suggest or contemplate splitting the memory clock signal into independent clock signals or in coupling those clock signals to the differing processing engines and selectively activating the independent clock signals. In fact, Jones teaches an opposite approach, namely a single variable frequency memory clock signal. It does not activate and deactivate multiple independent clock signals.

Houston is not directed to a memory clock source, graphics controller, or memory clock divider circuit and teaches away from the structure of Jones. Accordingly, these references are not properly combinable. Applicants respectfully note that there does not appear to be any stated motivation in the record to combine the opposite teachings of these references. Accordingly, Claim 1 is believed to be in condition for allowance.

As to Claim 2, Jones has been cited as teaching apparently two different clock sources as claimed, namely a memory clock source and an engine clock source. The Office Action cites item 5 of Fig. 1. However, Applicants respectfully submit that item 5 of Fig. 1 is the memory clock source that is not divided into independent clocks. There does not appear to be any teaching or suggestion of another engine clock source operatively coupled to a switching circuit to generate an output clock signal that is selectively coupled as a clock signal to a video overlay engine or video capture engine or any other graphics controller circuitry. Applicants respectfully request such a showing. In fact, it appears that Jones is silent as to a plurality of clocks as claimed. Accordingly, this claim is believed to be in condition for allowance.

As to Claim 3, Jones has been cited as teaching a variable memory clock control circuit operative to vary the speed of the memory clock based on the type of memory request from a plurality of memory requesters wherein the varying speed of the memory clock is passed through the memory clock divider circuit to generate a plurality of corresponding variable independent clock signals. However, Applicants respectfully reassert the relevant remarks made above with respect to Claim 1 and again note that Jones fails to teach or suggest independent clocks split

from the memory clock to processing engines and a variable memory clock control circuit that is operative to vary a speed of the memory clock and wherein the memory clock divider circuit divides the variable speed memory clock signals as a plurality of corresponding independent clock signals and selectively activates at least some of the plurality of independent clock signals in response to received condition data during an active mode. Accordingly, this claim is believed to be in condition for allowance.

As to Claim 7, the Office Action cites Fig. 4 of Jones as teaching that the memory clock divider circuit includes a plurality of logic circuits wherein each logic circuit outputs one of the plurality of corresponding independent clock signals and each logic circuit is coupled to operatively receive different condition data. However, Applicants again note that this is inconsistent with the previous position taken with respect to Fig. 1 wherein the Office Action admits that Jones "does not" show a plurality of corresponding independent clock signals to a number of interface circuits for differing processing engines. To the extent the Office Action is alleging that Jones teaches a memory clock divider circuit that generates divided memory clock output signals as a plurality of corresponding independent signals to a number of memory interface circuits for differing processing engines, Applicants respectfully reassert the relevant remarks made with respect to Claim 1.

Claims 4-6 and 8-16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Jones in view of Houston and further in view of U.S. Patent No. 5,544,101 (Houston '101). With respect to Claim 4, Applicants respectfully submit that the data stored by the claimed read latch has already been read from a memory device (e.g., such as Houston). The Houston '101 reference describes a memory device, such as a DRAM, that includes an internal memory array and multiplexer block and control block, wherein the memory device includes internal latch blocks operable to receive a plurality of input signals that are operable to retain a plurality of data states and operable to provide an output signal. Hence, this reference is directed to circuits internal to the memory. In contrast, Applicants' memory latch circuits and memory latch control circuits as claimed in Claim 4 are external to and not part of the memory device that receives the memory clock signal but instead are coupled to receive data from the memory device. Applicants also respectfully request factual support for any alleged motivation to combine the Houston references with one another and the Houston '101 reference with that of Jones.

Applicants respectfully submit that there is no suggestion or motivation to combine the teachings of the Houston references.

As to Claims 8-16, the Office Action indicates that these claims are rejected under the same rational discussed above in Claims 1-7. Accordingly, Applicants respectfully reassert the relevant remarks made above with respect to these claims.

Applicants respectfully submit that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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